WD_I, WD_{II} and WD_{III}, respectively, as shown in FIG. 15. The arbitrations I, II, and III produce Memory Grant signals MG_I, MG_{II} and MG_{III}, respectively, as indicated, for the registers 6204_I, 6204_{II} and 6204_{III}, respectively, of filter 6202_2 of logic section 5010_2, as shown in FIG. 18.

Thus, it should be noted that while each one of the registers 7002_1. 7002_2, 7002_3, of filters 6002_1, 6002_2 (FIGS. 19), are fed the same data from registers 7000_1, 7000_2, and 7000_3, respectively, because of the time skew shown in FIG. 18, such registers 7002_1. 7002_2, 7002_3, may not store the data which is in registers 7000_1, 7000_2, and 7000_3, respectively. However, the majority gates MG 7004_1-7004_3 will produce the same data according to FIG. 17. Therefore, the three abitrations I, II, and III of arbitration logic 6004_2 will receive the same data (i.e., the data produced by the majority gates MG 7004_1-7004_3) thereby providing coherency (i.e., synchronization) to the arbitrations I, II, and III even though the arbitrations are operating independently of each other.

Other embodiments are within the spirit and scope of the appended claims.

What is claimed is:

1. A method for checking the Cyclic Redundancy Cycle (CRC) of DATA, such DATA comprising a series of data words terminating in a CRC portion, such method comprising:

checking the CRC of the data words while delaying the DATA from passing to an output;

corrupting the delayed DATA if such checking determines a CRC error, such corruption of the DATA being performed prior to the data words pass to said output.

2. The method recited in claim 1 wherein the corrupting comprising corrupting a parity byte of such data words.

3. A system, comprising;

a source of DATA, such DATA comprising a series of bytes each byte having a parity bit, such series of bytes terminating in a Cyclic Redundancy Cycle (CRC) portion associated with the series of bytes of the DATA;

a source of a the CRC portion;

a CRC checker fed by the series of bytes of the DATA and the source of the CRC portion, for determining a CRC from the seines of bytes and for comparing such determined CRC with the CRC fed by the CRC source;

a delay fed by the series of bytes and the parity bits thereof;

a selector having a first input thereof fed by the parity bits and a second input thereof fed by the complement of such parity bits, such selector coupling the first input thereof to an output of such selector when the determined CRC is the same as the CRC fed by the CRC source and for coupling the second input thereof to the output when the determined CRC is different from the CRC fed by the CRC source, the output of the selector providing an appended parity bit for the data bytes after such data bytes pass through the delay.

4. A system, comprising;

a source of DATA, such DATA comprising a series of data words, each data word having a parity bit, each data word in the series being associated with a clock pulse,

such series of data words terminating in a Cyclic Redundancy Cycle (CRC) portion associated with the series of bytes of the DATA, such CRC portion comprising a predetermined number of CRC words, each one of such CRC words being associated with one of the clock pulses ;

a source of a the CRC portion;

a CRC checker fed by the series of data words and the source of the CRC portion, for determining a CRC from the seines of data words and for comparing such determined CRC with the CRC fed by the CRC source;

a delay fed by the series of DATA, such delay delaying the DATA by at least the number of CRC words;

a selector having a first input thereof fed by the parity bits and a second input thereof fed by the complement of such parity bits, such selector coupling the first input thereof to an output of such selector when the determined CRC is the same as the CRC fed by the CRC source and for coupling the second input thereof to the output when the determined CRC is different from the CRC fed by the CRC source, the output of the selector providing an appended parity bit for the data words after such DATA has passed through the delay.

5. The system recited in claim 4 including a second selector, such second selector having a first input fed the DATA and a second input fed by the output of the first-mentioned selector, such second selector coupling either the first input thereof or the second input thereof to an output of the second selector selectively in accordance with a control signal fed to such second selector.